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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/548,826	04/13/2000	David E. Charlton	4076US(99-01860)	7750

7590 05/04/2005

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EXAMINER	
BRITT, CYNTHIA H	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 05/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/548,826	CHARLTON ET AL.	
	Examiner	Art Unit	
	Cynthia Britt	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/14/05*.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *4/27/05*.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-19 are presented for examination.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on June 14, 2004 (resubmitted – see interview summary) has been considered by the examiner. Form 1449 has been signed and returned with this office action.

Drawings

The drawings were received on 6/14/04. These drawings are acceptable.

Specification/Preliminary Amendment

The preliminary amendment to the specification will be entered after the office receives an official copy. The examiner has reviewed an unofficial copy of the preliminary amendment.

Response to Arguments

Applicant's arguments filed June 14, 2004 have been fully considered but they are not persuasive.

Applicant argues: " As stated by the examiner, Faulk Jr. discloses 'a component with embedded memory,' which to a person of ordinary skill in the art implies a single device containing some memory along with other functions on the same device. In the

electronic arts and semiconductor industry, 'a component' is routinely used to denote an integrated circuit device. On the other hand, the present invention includes a 'plurality of memory devices' (i.e., components) as part of a 'memory module'."

The examiner disagrees with this statement. As it can be seen from, the Hiraki et al. reference (U.S. Patent No. 6,438,029) a memory module is used within a system on a chip (SOC) in a packaged integrated circuit.

Applicant also argues: "On the other hand, the present invention recited in claim 9, if for 'testing a memory module,' not a wafer, and the test information is stored 'on the memory module,' not on or in each individual device. As with the amendments to claims 1 and 5, Applicants have amended claim 9 to emphasize this distinction by clarifying the 'memory module' as a 'memory module including a memory module substrate and a plurality of memory devices disposed on the memory module substrate'."

The examiner would like to point out that IEEE defines a substrate as "the base material upon or within which an integrated circuit is fabricated or to which an integrated circuit is attached". Therefore, this limitation also fails to point out novelty in the instant application. It is unclear to the examiner why "testing a memory module" would be different than testing a memory wafer. The end result is that a memory is being tested and results are being stored in a nonvolatile memory. The examiner can see no difference in novelty between a circuit on a board, a card, or an integrated circuit as long as the functionality is the same.

Therefore, based on the newly inserted claim language, a new grounds of rejection is presented.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 are rejected under 35 U.S.C. 102(e) as being anticipated by Hiraki et al.

As per claim 1, Hiraki et al. teach the claimed memory module on a semiconductor integrated circuit device, over one semiconductor substrate: an electrically reprogrammable nonvolatile memory capable of being accessed by a control processing device, such as a central processing unit; and a volatile memory capable of being accessed by the control processing device, so that the stored information of the nonvolatile memory may be utilized for a connection change to effect a defect repair of the volatile memory. Specifically, the volatile memory includes: a plurality of first volatile memory cells, such as normal volatile memory cells, and a plurality of second volatile memory cells, such as redundancy volatile memory cells; and a volatile storage circuit for holding coupling control information for enabling the first volatile memory cells to be replaced by the second volatile memory cells. The nonvolatile memory includes a plurality of nonvolatile memory cells, some of which are used for storing coupling control information, so that the coupling control information is read out from the nonvolatile

memory cells and outputted by the reading and setting operations of the coupling control information, such as an instruction to initialize the semiconductor integrated circuit device. The volatile storage circuit is caused to fetch and store the coupling control information from the nonvolatile memory by the reading and setting operations. (Column 2 lines 35-40, column 3 lines 8-13 and lines 25-50, column 28 line 60 through column 29 line 23)

As per claim 2, Hiraki et al. teach the electrically reprogrammable nonvolatile memory should not be limited to a flash memory, but may adopt memory cells which include select MOS transistors and MNOS (Metal Nitride Oxide Semiconductor) storage transistors. The voltage applied states for programming and erasing the flash memory could be suitably modified. The nonvolatile memory may store information of multiple values such as four or more values. The volatile memory should not be limited to the SRAM or the DRAM but may be exemplified by a ferroelectric memory. (Column 27 lines 27-44)

As per claims 3 and 4, Hiraki et al. teach a testing process in which defective (failed) memory are identified and repaired, or are deemed fully functional (column 14 lines 24-65)

As per claim 5, Hiraki et al. teach the claimed memory module on a semiconductor integrated circuit device (a SOC), over one semiconductor substrate: an electrically reprogrammable nonvolatile memory capable of being accessed by a control processing device, such as a central processing unit; and a volatile memory capable of being accessed by the control processing device, so that the stored information of the

nonvolatile memory may be utilized for a connection change to effect a defect repair of the volatile memory. Specifically, the volatile memory includes: a plurality of first volatile memory cells, such as normal volatile memory cells, and a plurality of second volatile memory cells, such as redundancy volatile memory cells; and a volatile storage circuit for holding coupling control information for enabling the first volatile memory cells to be replaced by the second volatile memory cells. The nonvolatile memory includes a plurality of nonvolatile memory cells, some of which are used for storing coupling control information, so that the coupling control information is read out from the nonvolatile memory cells and outputted by the reading and setting operations of the coupling control information, such as an instruction to initialize the semiconductor integrated circuit device. The volatile storage circuit is caused to fetch and store the coupling control information from the nonvolatile memory by the reading and setting operations. (Abstract, column 2 lines 35-40, column 3 lines 8-13 and lines 25-50, column 6 lines 36-65, column 28 line 60 through column 29 line 23)

As per claim 6, Hiraki et al. teach the electrically reprogrammable nonvolatile memory should not be limited to a flash memory, but may adopt memory cells which include select MOS transistors and MNOS (Metal Nitride Oxide Semiconductor) storage transistors. The voltage applied states for programming and erasing the flash memory could be suitably modified. The nonvolatile memory may store information of multiple values such as four or more values. The volatile memory should not be limited to the SRAM or the DRAM but may be exemplified by a ferroelectric memory. (Column 27 lines 27-44)

As per claims 7 and 8, Hiraki et al. teach a testing process in which defective (failed) memory are identified and repaired, or are deemed fully functional (column 14 lines 24-65)

As per claim 9, Hiraki et al. teach the claimed testing process in which defective (failed) memory are identified and repaired, or are deemed fully functional (column 14 lines 24-65) and the claimed memory module on a semiconductor integrated circuit device, over one semiconductor substrate: an electrically reprogrammable nonvolatile memory capable of being accessed by a control processing device, such as a central processing unit; and a volatile memory capable of being accessed by the control processing device, so that the stored information of the nonvolatile memory may be utilized for a connection change to effect a defect repair of the volatile memory. Specifically, the volatile memory includes: a plurality of first volatile memory cells, such as normal volatile memory cells, and a plurality of second volatile memory cells, such as redundancy volatile memory cells; and a volatile storage circuit for holding coupling control information for enabling the first volatile memory cells to be replaced by the second volatile memory cells. The nonvolatile memory includes a plurality of nonvolatile memory cells, some of which are used for storing coupling control information, so that the coupling control information is read out from the nonvolatile memory cells and outputted by the reading and setting operations of the coupling control information, such as an instruction to initialize the semiconductor integrated circuit device. The volatile storage circuit is caused to fetch and store the coupling control information from the

nonvolatile memory by the reading and setting operations. (Column 2 lines 35-40, column 3 lines 8-13 and lines 25-50, column 28 line 60 through column 29 line 23)

As per claims 10 and 11, Hiraki et al. teach the nonvolatile memory includes a plurality of nonvolatile memory cells, some of which are used for storing coupling control information, so that the coupling control information is read out from the nonvolatile memory cells and outputted by the reading and setting operations of the coupling control information, such as an instruction to initialize the semiconductor integrated circuit device. The volatile storage circuit is caused to fetch and store the coupling control information from the nonvolatile memory by the reading and setting operations. (Column 3 lines 25-50, column 14 lines 24-65)

As per claim 12, Hiraki et al. teach the electrically reprogrammable nonvolatile memory should not be limited to a flash memory, but may adopt memory cells which include select MOS transistors and MNOS (Metal Nitride Oxide Semiconductor) storage transistors. The voltage applied states for programming and erasing the flash memory could be suitably modified. The nonvolatile memory may store information of multiple values such as four or more values. The volatile memory should not be limited to the SRAM or the DRAM but may be exemplified by a ferroelectric memory. (Column 27 lines 27-44)

As per claims 13 and 14, Hiraki et al. teach the claimed testing process in which defective (failed) memory are identified and repaired, or are deemed fully functional (column 14 lines 24-65) and the claimed memory module on a semiconductor integrated circuit device, over one semiconductor substrate: an electrically reprogrammable

nonvolatile memory capable of being accessed by a control processing device, such as a central processing unit; and a volatile memory capable of being accessed by the control processing device, so that the stored information of the nonvolatile memory may be utilized for a connection change to effect a defect repair of the volatile memory. (Column 2 lines 35-40, column 3 line 51 through column 4 line 9, column 28 line 60 through column 29 line 23)

As per claim 15, Hiraki et al. teach the claimed (fabrication process column 4 lines 9-52) fabrication of a memory module on a semiconductor integrated circuit device (a SOC), over one semiconductor substrate: an electrically reprogrammable nonvolatile memory capable of being accessed by a control processing device, such as a central processing unit; and a volatile memory capable of being accessed by the control processing device, so that the stored information of the nonvolatile memory may be utilized for a connection change to effect a defect repair of the volatile memory. Specifically, the volatile memory includes: a plurality of first volatile memory cells, such as normal volatile memory cells, and a plurality of second volatile memory cells, such as redundancy volatile memory cells; and a volatile storage circuit for holding coupling control information for enabling the first volatile memory cells to be replaced by the second volatile memory cells. The nonvolatile memory includes a plurality of nonvolatile memory cells, some of which are used for storing coupling control information, so that the coupling control information is read out from the nonvolatile memory cells and outputted by the reading and setting operations of the coupling control information, such as an instruction to initialize the semiconductor integrated circuit device. The volatile

storage circuit is caused to fetch and store the coupling control information from the nonvolatile memory by the reading and setting operations. (Abstract, column 2 lines 35-40, column 3 lines 8-13 and lines 25-50, column 6 lines 36-65, column 28 line 60 through column 29 line 23) Hiraki et al. also teach a testing process in which defective (failed) memory are identified and repaired, or are deemed fully functional (column 14 lines 24-65)

As per claims 16-19, Hiraki et al. also teach the defect repairs of the DRAM and the SRAM can be performed, as exemplified in, first of all, on the result of a first probe inspection of a chip, which was manufactured in the wafer process by the maker of the microcomputer. In the repair at this time, the microcomputer is brought into the EPROM writer mode by the mode bit so that the flash memory can be accessed by using a dedicated write device, such as a tester or an EPROM writer, and the mode bit is set to the logic value "O" to write the repair information in a predetermined region of the flash memory. After this, the probe inspection is performed again), and a screening is performed by way of a packaging and a burn-in test for testing the reliability by making the power voltage Vdd higher than that of the ordinary operation. A chance for repairing a defect can be given to the article, which was newly found to be defective, the burn-in test. When a defect is actualized by the burn-in test in the microcomputer, which was not found defective at Step S2, for example, it can be repaired like before. The defect-repaired article is screened again and is then shipped. The user having purchased that article assembles the microcomputer with a desired circuit substrate, so that the assembled circuit is suitably operated. If necessary, to execute a defect diagnosing test

program (or diagnostic program) to decide whether or not a defect exists and whether the defect can be repaired (at S11), if discovered, in the on-board state through the CPU, which is packaged in the microcomputer. For example, either a defect, which has developed as a microcomputer having no defect in the manufacturing process is aged to deteriorate its circuit elements or circuit factors, or a new defect, which is developed according to changes in the operating environments such as the operating temperature or the operating voltage, can be repaired. The diagnostic program for repairing of defects due to the on-board write operation and the write program to be executed at the on-board programming time can be stored in regions other than the word line of the flash memory. The diagnostic programs could be automatically executed either by instructing the CPU arbitrarily by an interruption or by using a timer. Although the content of the diagnostic program is not shown in detail, it performs the operations to write a predetermined test pattern in the SRAM and the DRAM and read it, to determine the existence of a defect by comparing the read data and expected value data, and to inspect, if a defect is detected, whether or not a repairable redundancy construction is left. When the repairable redundancy construction is left, the CPU is caused to execute the write program thereby to write the repair information in a predetermined memory cell of the flash memory so that the repair information for repairing the defect may be programmed in the repair information storing nonvolatile memory cell of the flash memory. (FIG. 4(A) 4(B), column 14 lines 24-65, column 28 line 60 through column 29 line 23)

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Cynthia Britt
Examiner
Art Unit 2133

GUY LAMARRE
PRIMARY EXAMINER

OK
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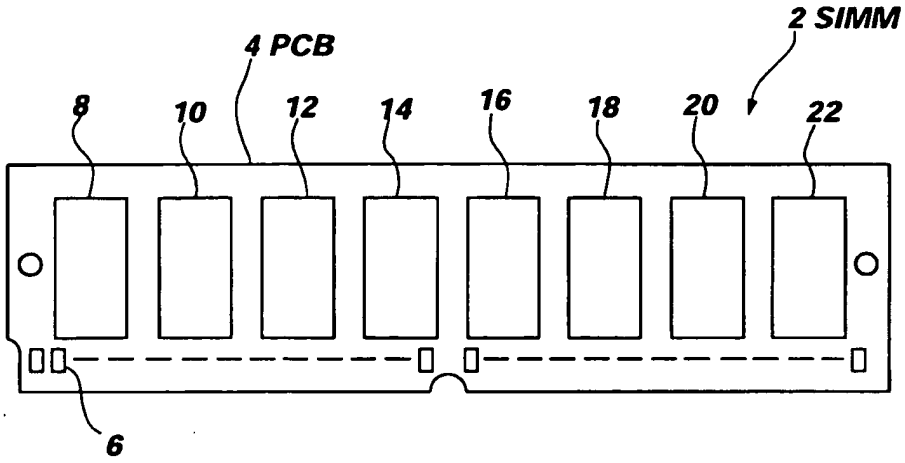

Fig. 1
(PRIOR ART)

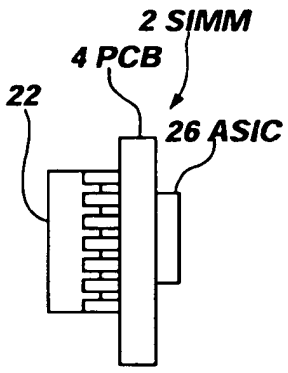

Fig. 2
(PRIOR ART)

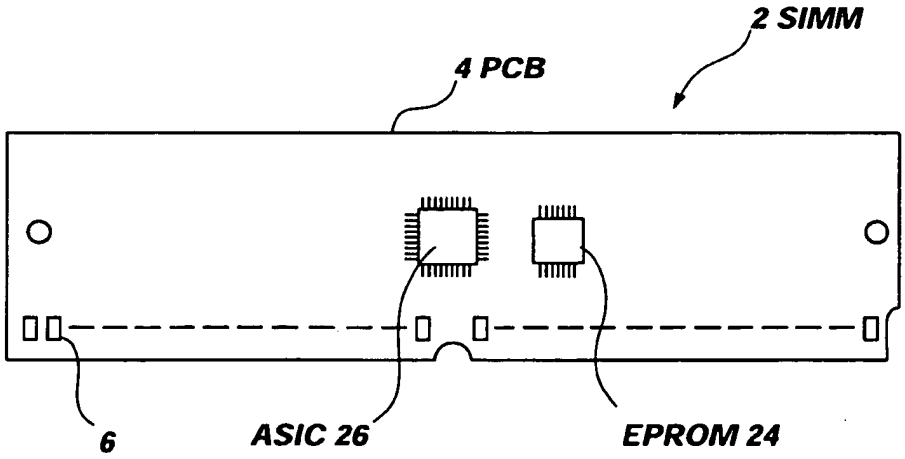

Fig. 3
(PRIOR ART)

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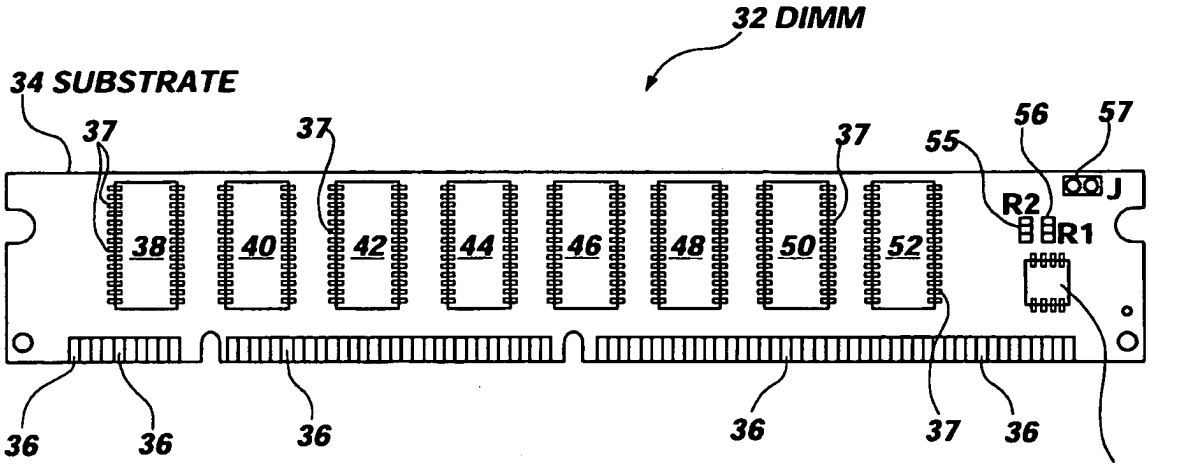

Fig. 4

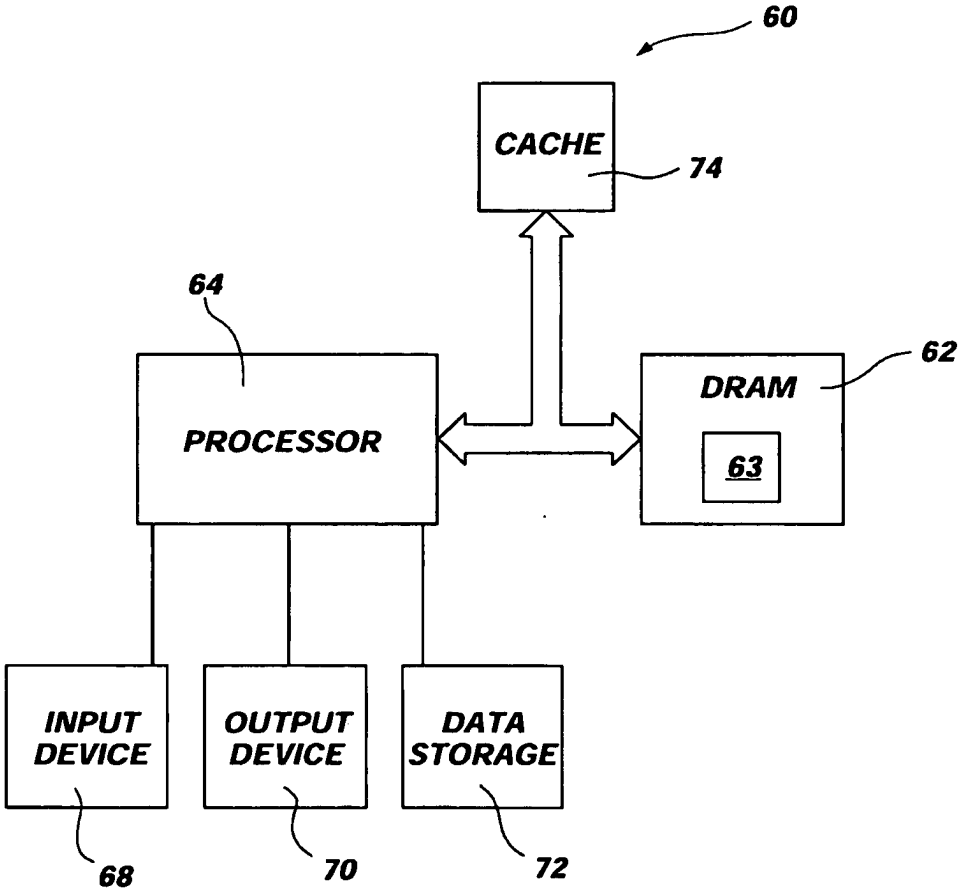

Fig. 5